AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings include a new FIG. 5. These three sheets, which include FIGS. 1 -5, replace the two prior sheets, which included FIGS. 1-4.

Attachments: One .pdf file containing three replacement sheets

REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove.

Claims 1-29 are pending. Claims 1-4, 6-16, and 18-29 are rejected and Claims 5 and 17 are withdrawn from consideration. Claims 1, 14, and 24 are amended hereinabove.

In response to the drawing objection, the Specification has been amended and FIG. 5 has been added hereinabove.

Amended independent Claim 1 positively recites that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

The Applicant notes that the Office Action (pages 3-4) points to the voltage supply being dependent on the transistor parameters in the diode-bridged footer. The Applicant submits that what is advantageously claimed is

voltage supply based on the transistor parameters of the memory cell, not based on the transistor parameters of the supply circuit (see the Specification paragraphs 0029-0030, 0036-0037 and 0040).

Regarding Claim 2, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n -well voltage at about high operating voltage VDD of 1.2 V" does not teach that V_{ADD} is set relative to a well voltage.

Regarding Claim 3, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n -well voltage at about high operating voltage VDD of 1.2 V" does not teach that V_{ASS} is set relative to a well voltage.

Regarding Claim 4, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n -well voltage at about high operating voltage VDD of 1.2 V" does not teach a well voltage at about V_{DD} during sleep mode.

Regarding Claim 8, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n -well voltage at about high operating voltage VDD of 1.2 V" does not teach the sleep mode voltage controller further provides a well voltage and the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltages provided as a set of optimum values for a general technology class of transistors.

Regarding Claim 9, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n -well voltage at about high operating voltage VDD of 1.2 V" does not teach that the sleep mode voltage controller adjusts the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a sleep mode current.

Regarding Claim 10, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n -well voltage at about high operating voltage VDD of 1.2 V" does not teach that the sleep mode voltage controller refines the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current.

Regarding Claim 9, the Applicant respectfully submits that the statement in the Office Action (page 4) that "sleep mode current (see lines 56 -67, column 3; line 28, column 7; lines 37 -38, column 8)" does not teach that sleep mode voltage controller adjusts the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a sleep mode current . Choosing the boundary between voltage regions to minimize leakage current at the boundary (column 3 lines 52-67) does not teach choosing the voltage based on leakage current.

Regarding Claim 10, the Applicant respectfully submits that the statement in the Office Action (page 4) that "sleep mode current (see lines 56 -67, column 3; line 28, column 7; lines 37 -38, column 8)" does not teach that the sleep mode voltage controller refines the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current . Choosing the boundary between voltage regions to minimize leakage current at the boundary (column 3 lines 52-67) does not teach choosing the voltage based on leakage current.

Regarding Claim 13, the Applicant respectfully submits that the statement in the Office Action (page 4) that "retention data (see lines 30 -31, column 2)" does not teach that the sleep mode voltage control ler provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across the SRAM array that is sufficient for data retention and minimizing a total leakage current . Deng et al. does not teach minimizing leak age current while retaining data (column 2 lines 27-31).

Regarding Claim 11, the Applicant respectfully submits that the statement in the Office Action (page 4) that " power down voltage controller 170 providing the same n well bias (see lines 41 -42, column 6) at 1.2 volts for the n -well of the SRAM array 110 (see lines 31 -34, column 6) and the voltage across the SRAM cell can be decreased to 1.2 volts (see lines 22 -28, column 6)." does not teach that the sleep mode voltage controller further provides a well voltage such that an

n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage. Deng et al. does not teach the voltages are approximately equal, rather Deng et al. teaches V_{nwell} can equal to V_{ADD} (column 5 lines 16-42) – which isn't pertinent to the advantageously claimed invention.

Regarding Claim 3, the Applicant respectfully traverses the statement in the Office Action (page 5) that "since the SRAM array 110 does have n-well, therefore, it also inherently must have a substrate at a voltage which also inherently must be equivalent to the low operating supply voltage Vss as well known in the art." The Applicant submits that it is well known in the art to have a substrate voltage different than V_{SS} (to adjust for variations in the threshold voltage caused by process variations). In some applications V_{SS} is routed separate from the substrate voltage so that the back bias can be applied to the NMOS transistors. (See also FIG. 2.)

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 1 and respectfully asserts that Claim 1 is patentable over Deng et al. Furthermore, Claims 2-4 and 6-13 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the reference of record.

Amended independent Claim 14 positively recites that providing the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} is based on a transistor parameter of at least one transistor of the SRAM array. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

The Applicant notes that the Office Action (pages 3-4) points to the voltage supply being dependent on the transistor parameters in the diode-bridged footer. The Applicant submits that what is advantageously claimed is voltage supply based on the transistor parameters of the memory cell, not based on the transistor parameters of the supply circuit (see the Specification paragraphs 0029-0030, 0036-0037 and 0040).

Regarding Claim 15, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n-well voltage at about high operating voltage VDD of 1.2 V" does not teach that V_{ADD} is set relative to a well voltage.

Regarding Claim 16, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n-well voltage at about high operating voltage VDD of 1.2 V" does not teach a well voltage at about V_{DD} during sleep mode.

Regarding Claim 21, the Applicant respectfully submits that the statement in the Office Action (page 4) that "sleep mode current (see lines 56-67, column 3; line 28, column 7; lines 37-38, column 8)" does not teach adjusting the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a sleep mode current. Choosing the boundary between voltage regions to minimize leakage current at the boundary (column 3 lines 52 -67) does not teach choosing the voltage based on leakage current.

Regarding Claim 22, the Applicant respectfully submits that the statement in the Office Action (page 4) that "sleep mode current (see lines 56-67, column 3; line 28, column 7; lines 37-38, column 8)" does not teach refining the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a diode leakage current. Choosing the boundary between voltage regions to minimize leakage current at the boundary (column 3 lines 52 -67) does not teach choosing the voltage based on leakage current.

Regarding Claim 23, the Applicant respectfully submits that the statement in the Office Action (page 4) that "power down voltage controller 170 providing the same n well bias (see lines 41-42, column 6) at 1.2 volts for the n-well of the SRAM array 110 (see lines 31-34, column 6) and the voltage across the SRAM cell can be decreased to 1.2 volts (see lines 22 -28, column 6)." does not teach providing a well voltage such that an n-channel back bias voltage, a p-channel

back bias voltage and a voltage across a SRAM cell are all about a same voltage. Deng et al. does not teach the voltages are approximately equal, rather Deng et al. teaches V_{nwell} can equal to V_{ADD} (column 5 lines 16-42) – which isn't pertinent to the advantageously claimed invention.

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 14 and respectfully asserts that Claim 14 is patentable over Deng et al. Furthermore, Claims 15-16 and 18-23 are allowable for depending on allowable independent Claim 14 and, in combination, including limitations not taught or described in the reference of record.

Amended independent Claim 24 positively recites that sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are based on a transistor parameter of at least one transistor of the SRAM array. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

The Applicant notes that the Office Action (pages 3-4) points to the voltage supply being dependent on the transistor parameters in the diode-bridged footer. The Applicant submits that what is advantageously claimed is voltage supply based on the transistor parameters of the memory cell, not based

on the transistor parameters of the supply circuit (see the Specification paragraphs 0029-0030, 0036-0037 and 0040).

Regarding Claim 25, the Applicant respectfully submits that the statement in the Office Action (page 4) tha t "retention data (see lines 30 -31, column 2)" does not teach that the sleep mode voltage controller performs the modify based on reducing current leakage of the SRAM array and providing sufficient voltage across the SRAM array via the array high supply vo ltage V_{ADD} and the array low supply voltage V_{ASS} to retain data . Deng et al. does not teach reducing leakage current while retaining data (column 2 lines 27-31).

Regarding Claim 27, the Applicant respectfully traverses the statement in the Office Action (page 5) that "since the SRAM array 110 does have n -well, therefore, it also inherently must have a substrate at a voltage which also inherently must be equivalent to the low operating supply voltage Vss as well known in the art." The Applicant submits t hat it is well known in the art to have a substrate voltage different than V_{SS} (to adjust for variations in the threshold voltage caused by process variations). In some applications V_{SS} is routed separate from the substrate voltage so that the back bias c an be applied to the NMOS transistors. (See also FIG. 2.)

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 24 and respectfully asserts that Claim 24 is patentable over Deng et al. Furthermore, Claims 25-29 are allowable for depending on allowable independent Claim 24 and, in combination, including limitations not taught or described in the reference of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

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